

ABSTRACT

An integrated digital subscriber line transceiver includes a single integrated circuit that has a digital signal processing engine, a time division multiplexing framer (for example, a T1/E1 framer), and a static random access memory. The integrated circuit also includes a microprocessor coupled to the digital signal processing engine, the time division multiplexing framer, and the static random access memory. The digital signal processing engine, in one embodiment, includes an HDSL2/G.SHDSL data pump and an HDSL2/G.SHDSL framer.